REMARKS

The claims are claims 1, 4, 5, 9 to 11, 13, 16 and 17.

Claims 2, 3, 6 to 8, 12, 14, 15 and 18 to 24 are canceled. Claims 18 to 24 are newly canceled.

Claims 1, 4, 5, 10, 11, 13, 16 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al. Pub. No. US 2003/0088601 Al and Adelman et al. U.S. Patent No. 5,666,300.

Claims 1 and 13 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 1 recites "combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." This recitation of the mid-position carry input for rounding represents subject matter neither taught in nor made obvious by the references. The OFFICE ACTION states at page 2, line 23 to page 3, line 6 that Pitsianis et al discloses:

> "rounding (627) the combined product to form an intermediate result via an arithmetic circuit (627) having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result (Figure 2B with rounding architecture and col. 3 0049-0054 wherein the carry-input is a rounding factor according to conventional rounding architecture as ROUND, TRUNC, CEIL, or FLOOR and in Figure 3B the shifting/dividing is done prior rounding)"

While the OFFICE ACTION states that this is disclosed in Pitsianis et al, in fact neither subtractor 623, adder 625, rounder circuit 627 of Figure 6 nor adder 723, subtractor 725 nor rounder 737 illustrate the "mid-position carry input" recited in claims 1 and 13. The cited test of paragraphs [0049] to [0054] disclose rounding modes without disclosing the recited "mid-position carry input." The Applicants respectfully submit that Pitsianis et al includes no disclosure of a mid-position input and no disclosure of a carry input. Accordingly, claims 1 and 13 are not made obvious by the combination of Pitsianis et al and Adelman et al.

Claims 16 and 17 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 16 recites "the step of shifting further includes sign extending the intermediate result." Claim 17 recites the shifter "sign extends the output of the arithmetic circuit." The OFFICE ACTION cites rounder circuit 627 illustrated in Figure 6 of Pitsianis et al as disclosing this element in "selecting only 30-15 out of 32 bits." The Applicant respectfully submits this is in error. "Sign extending" and "sign extend" are terms known in the art. A signed number has a most significant bit indicating the sign. A "0" indicates a positive number while a "1" indicates a negative number. Sign extension duplicates this most significant bit to maintain the sign indication following the shift operation. Pitsianis et al include no such disclosure. In fact, Pitsianis et al includes no teaching of signed numbers and therefore cannot teach the claimed sign extension. Accordingly, claims 16 and 17 are allowable over the combination of Pitsianis et al and Adelman et al.

Claims 4, 5 and 9 to 11 are allowable by dependence upon respective allowable base claims 1 and 13.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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